HTD1K5N10 P-1

30V N-Ch Power MOSFET

V_{DS}		100	V
$R_{DS(on),typ}$	V_{GS}=10V	130	mΩ
$I_{D\ (Sillicon\ Limited)}$		10	A

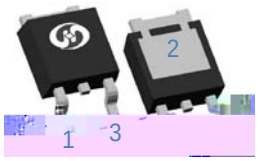
Feature

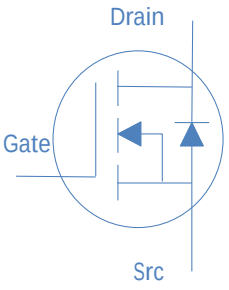
- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Application

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial

TO-252





Part Number	Package	Marking
HTD1K5N10	TO-252	TD1K5N10

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	10	A
		T_C=100	7	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	40	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	7	mJ
Power Dissipation	P_D	T_C=25	35	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	4.2	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	2.0	3	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=80V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=70V, T_j=125	-	-	25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	-	130	150	mΩ
		V_{GS}=5V, I_D=10A	-	150	175	
Transconductance	g_{fs}	V_{DS}=5V, I_D=10A	-	8	-	S
Gate Resistance	R_G	V_{GS}=15mV, V_{DS} =0V, f=1MHz	-	2.0	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	1070	-	pF
Output Capacitance	C_{oss}		-	52	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Total Gate Charge	Q_g(10V)	V_{DD}=80V, I_D=10A, V_{GS}=10V	-	18.8	-	nC
Gate to Source Charge	Q_{gs}		-	3.8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=1A, V_{GS}=10V, R_G=6Ω,	-	15	-	ns
Rise time	t_r		-	35	-	
Turn off Delay Time	$t_{d(off)}$		-	25	-	
Fall Time	t_f		-	25	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=10A	-		1.3	V
Reverse Recovery Time	t_{rr}	I_F=10A, dI_F/dt=100A/μs	-	120	-	ns
Reverse Recovery Charge	Q_{rr}		-	520	-	nC

Fig 1. Typical Output Characteristics

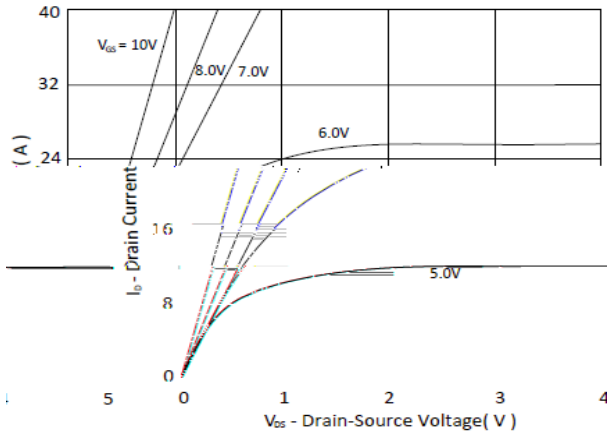


Figure 2. On-Resistance vs. Gate-Source Voltage

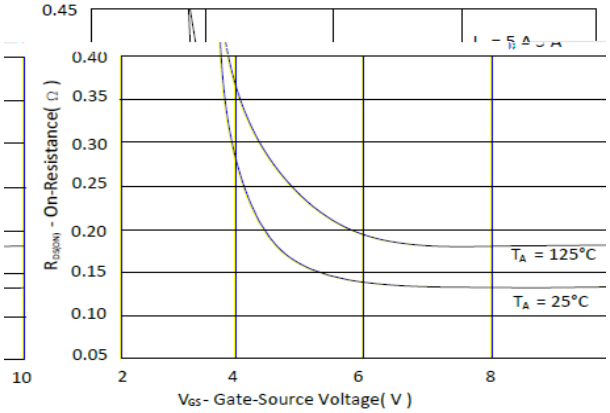


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

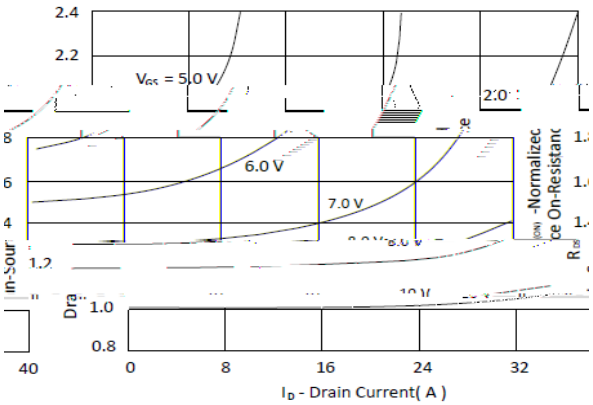


Figure 4. Normalized On-Resistance vs. Junction Temperature

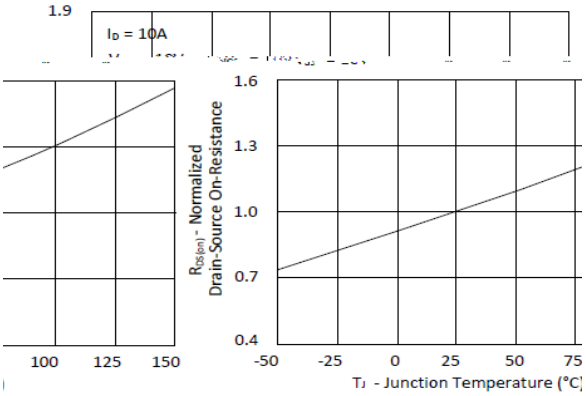


Figure 5. Typical Transfer Characteristics

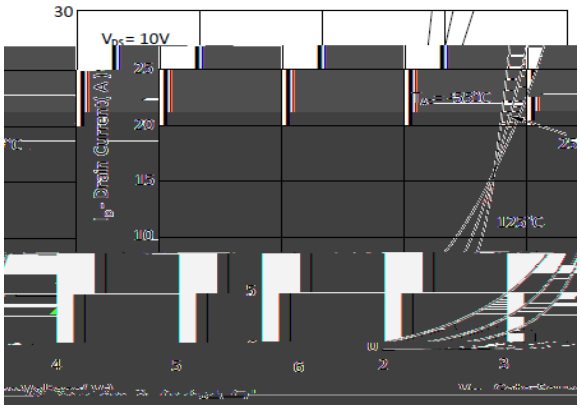


Figure 6. Typical Source-Drain Diode Forward Voltage

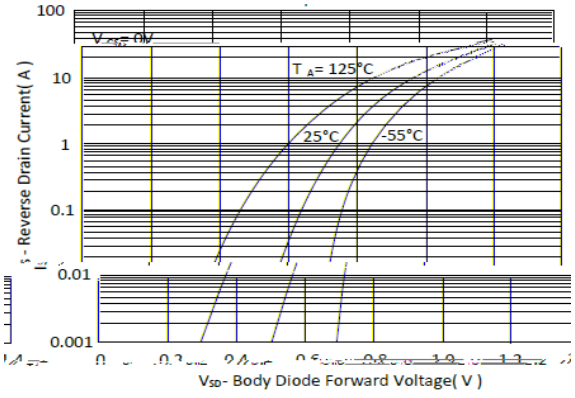


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

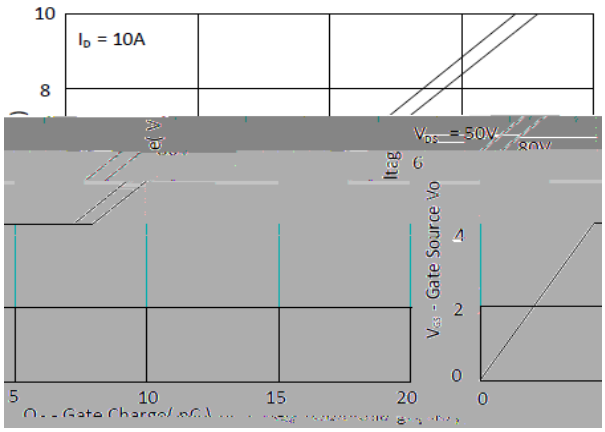


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

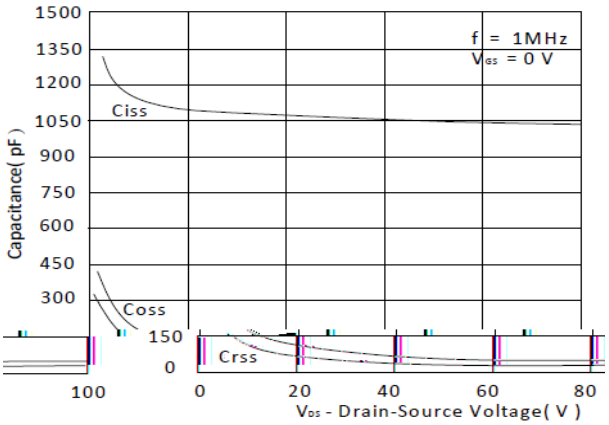


Figure 9. Maximum Safe Operating Area

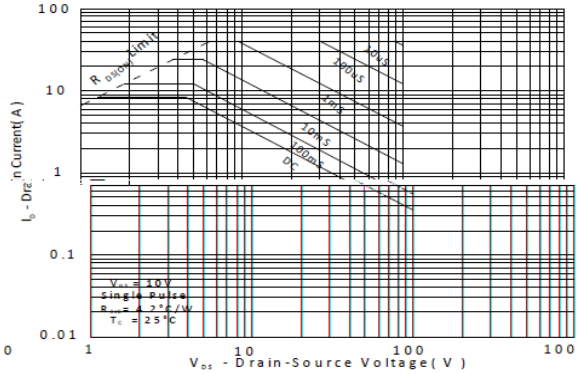


Figure 10. Single Pulse Maximum Power Dissipation

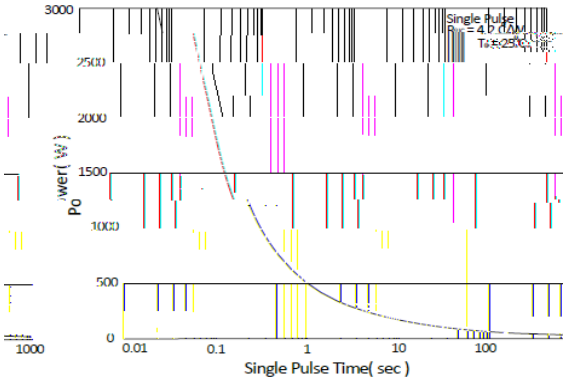
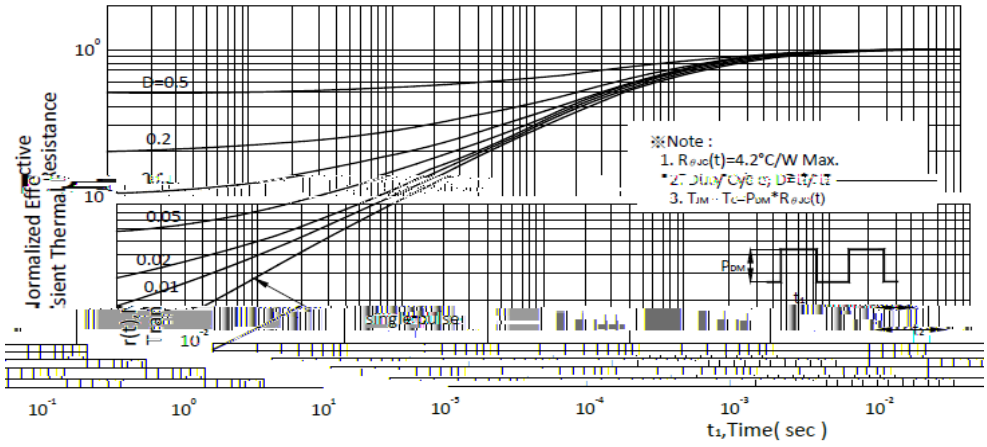
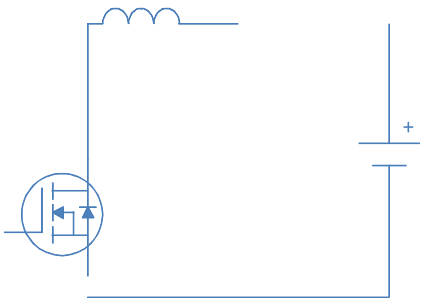


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Inductive switching Test	

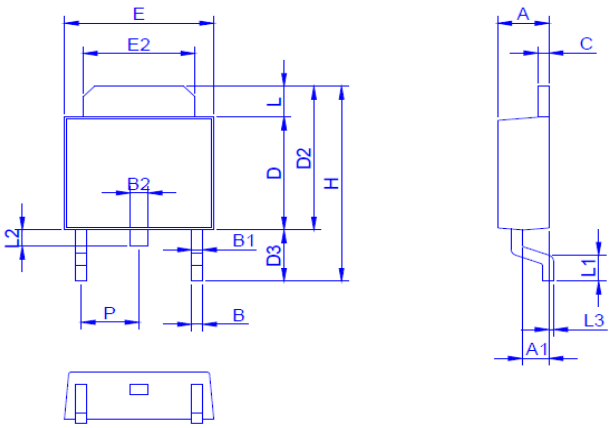
Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

TO-252, 3leads



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50